ANALYSIS OF MICROVIA INTERCONNECTS

Ramesh Abhari and T.E. van Deventer

Department of Electrical and Computer Engineering
University of Toronto, 10 King's College Road, Ontario M5S 3G4, CANADA

Abstract

The development of high density circuitry has promoted the introduction of the microvia technology which relies on organic dielectrics and vertical interconnects of reduced dimensions. In this paper, microvia interconnects are evaluated both through simulation using an FDTD model and experimental measurements, and have shown good electrical performance.

I. INTRODUCTION

Presently, new technologies for electronic packaging are being developed by original equipment manufacturers (OEM) in the telecommunication and computer industry to meet the increasing demand for compact circuits in mobile electronics and hand-held products. The need for denser, smaller and lighter boards has promoted the use of high density ICs with large number of I/O pins, such as multichip modules (MCMs) or flip chip on board (FCOB) assemblies. To accommodate the resulting localized higher interconnect densities, microvia substrates with reduced geometries have been introduced which combine conventional multilayer printed circuit board technologies with new advanced technologies [1].

These microvia layers, which feature a small overall via profile, are implemented within an organic substrate on either or both sides of a rigid laminate substrate using photodefined, plasma etched or laser ablated technologies. Since these microvias are embedded in inhomogeneous environments, they can potentially suffer from dispersion, while the interconnecting lines deposited on the thin dielectric layers may be prone to broadside coupling or crosstalk (Figure 1).

In this paper, characterization of these microvias is performed using a Finite Difference Time Domain (FDTD) fullwave technique. Validation is achieved through a set of experimental measurements using TDR and network analyzer setups.

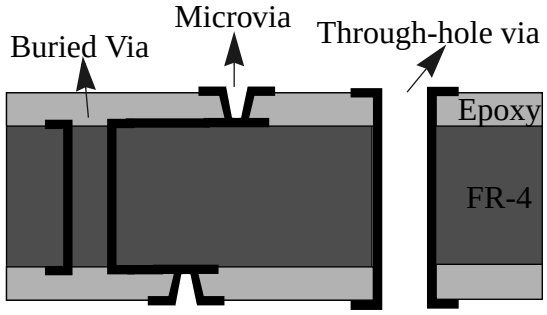

Figure 1 - Cross-section view of a typical PCB containing microvias and through-hole vias

II. MICROVIA SIMULATION

The Finite Difference Time Domain (FDTD) method has been successfully applied to the analysis of planar and vertical interconnects over the past few years [2-4]. In this work, this method is directed to the study of single and multiple microvias excited by a gaussian pulse of amplitude 1V/m and variable width. The geometry, shown in Figure 1, includes an FR-4 layer

0-7803-4471-5/98/$10.00 (c) 1998 IEEE

sandwiched between two layers of epoxy coated copper foils. Plasma etching technology allows manufacturing of microvias of diameter between 3 to 6 mils as opposed to conventional mechanically drilled through-hole vias with 12 mils diameter or larger. The surface pad diameter of a typical microvia is 12 mils, i.e. about 60 percent smaller than that of a through-hole via. In turn, signal traces of width between 3 to 5 mils are matched at both ends. In the simulation, the thickness of the epoxy layers is 1.5 mils while that of the FR-4 is 20 mils.

Single microvia*:* The microvia is represented as a straight square metallic post of negligible thickness. The effect of the inhomogeneous dielectric (Epoxy/FR-4) is shown waveform to provide only minor reflection in the reflected (Figure 2). From the time domain simulation, the scattering parameters are extracted and a geometry-dependent equivalent circuit derived.

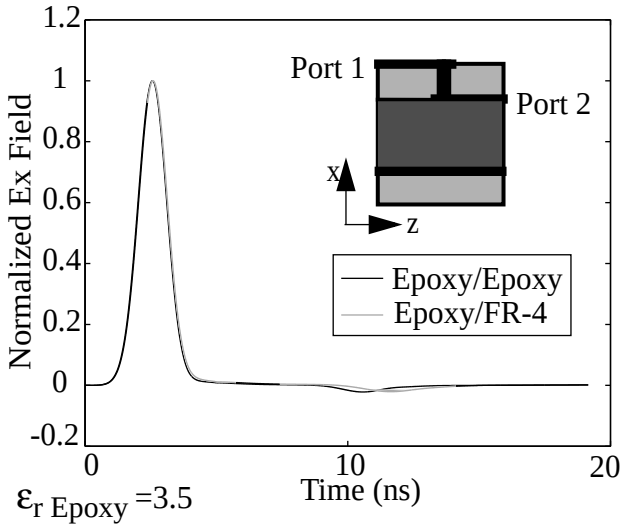

Figure 2 - Time domain waveform at Port 1 for a single microvia in a 3-layer board

Multiple microvias: To investigate the electrical behavior of multiple microvias, the circuit shown as Structure A in Fig. 3(a) is modeled using the FDTD method. Structure A consists of two microvias connected with microstrip lines on the top layer and an embedded line on interface 2. The high/low/high impedance transition is identified in Figure 3(b) by the sign of the reflected waveform, which tends to overwhelm the reflections due to the microvias.

Ground plane placement: The high density of interconnects to be routed locally requires the use of multiple layers, potentially exposing the lines to broadside coupling or crosstalk. To address this potential problem, ground plane placement within the multilayer board is closely examined for the different configurations shown in Figure 3(a). While the added ground plane on interface 2 (Structure B) reduces dispersion by essentially eliminating the Epoxy/FR-4 interface, it does affects the signal which travels along the microstrip lines on surface 1 and the conductor-backed coplanar line between the microvias on interface 2. This low/high/low impedance transition translates into larger and reverse multiple reflections compared to structure A. For Structure C with a ground plane on interface 2 only, an overall similar reflected signature is observed. The size of the ground clearance, chosen here as 60 x 24 mils, also affects signal integrity.

From the time domain simulation results, the scattering parameters are determined as shown in Figure 3(c) where S_{11} shows a minimum near 30 GHz when *d* is about a half wavelength, resulting in a series resonant circuit behavior.

III. MEASUREMENTS

Measurements were performed on the test vehicle shown in Figure 4 which was manufactured by Merix Corporation. This multilayer board has a single microvia layer fabricated with plasma etched technology. The vias are connected by lines on a 2 mil polyimide dielectric backed by a 15-mil epoxy FR-4 layer. The design of the test structures is duplicated on the coupon: one half has the ground planes on inter-

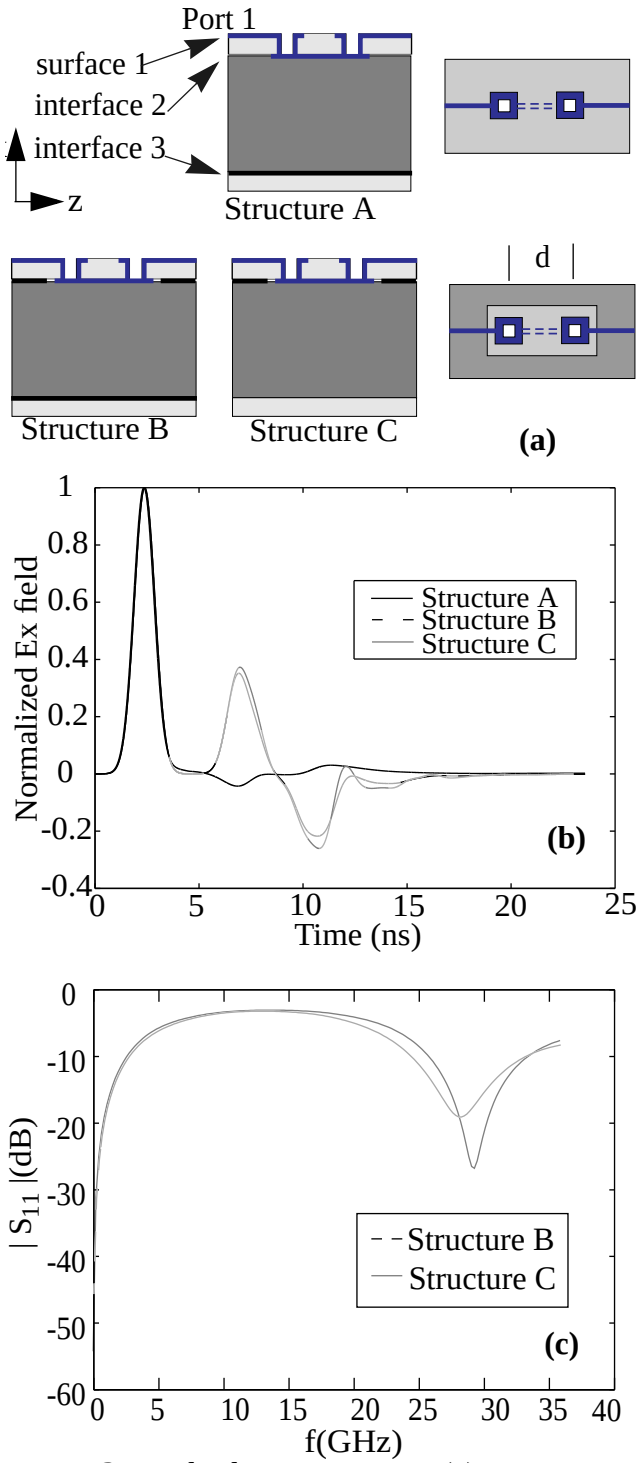

Figure 3 - Multiple via structures (a) geometries with different ground plane placement, (b) time domain waveform at Port 1, (c) S_{11} parameter for Structures B and C

faces 2 and 3, while the other half has the ground plane on interface 3 only, which correspond to Structures B and A of the previous section, respectively. The board therefore provides a useful platform for validating the effect of a single microvia, multiple microvias and the ground plane positioning on signal degradation.

In this paper, we concentrate on structures 5 and 12 (Figure 4) representing a circuit trace with a microvia in the middle of the circuit and half of the trace on interface 2, and structures 6 and 11 which represent a daisy chain of vias with both endpoints on surface 1. Structures 3 and 4 are through lines on surface 1 and interface 2, respectively, and structures 13 and 14 are their mirror images. These structures provide a simple means of validating the line impedance calculations using a Time Domain Reflectometry (TDR) set-up, with a 40 *ps* risetime step excitation.

All structures were tested in both frequency and time domain. The network analyzer results shown in Figure 5(a) illustrate the S_{11} frequency behavior, where the dips for Structure 5 can be traced back to the even harmonics of structures 3 and 4. The reflected waveform for a single via on Figure 5(b) clearly shows the mismatch between the 50 Ω connections and the microstrip line on layer 1 (47 Ω for Structure 5 and 115 Ω for Structure 12). For the daisy chain of 40 vias, an average characteristic impedance (76 Ω for Structure 6 and 101 Ω for Structure 11) can be observed in Figure 5(c). The peak reflections in the response for Structure 6 stem again from the impedance mismatch between the TDR connectors and the microstrip lines on layer 1.

IV. CONCLUSIONS

While still at the evaluation stage by OEMs, the preliminary results from simulation and measurements presented herein show that microvias exhibit desirable electrical performance and low reflections in multilayered circuits, while providing a viable means of addressing high density

circuitry. Lumped-element models for the different geometries discussed will be presented at the conference.

ACKNOWLEDGEMENTS

This work was supported by Nortel Technology, the Information Technology Research Centre Ontario, and the Bell Canada/NSERC Industrial Research Chair in Electromagnetics.

REFERENCES

[1] G. Brist, J. Sewart, S. Bird, "Plasma-etched microvias", *Printed Circuit Fabrication Journal*, vol. 20, pp.34-37, 1997

[2] J. Yook, N.I. Dib, L. Katehi, "Characterization of high frequency interconnects using finite difference time domain and finite element methods," *IEEE Trans. Microwave Theory Tech.*, vol. 42, pp. 1727-1736, Sept. 1994.

[3 D.M. Sheen, S.M. Ali, M.D. Abouzahra, and J.A. Kong, "Application of the three-dimensional finite-difference time-domain method to the analysis of planar microstrip circuits," *IEEE Trans. Microwave Theory Tech.*, vol. 38, pp. 849-857, July 1990.

[4] E. Pillai, "A technique to reduce crosstalk and enhance impedance match at vias in high-frequency multilayer packages verified by FDTD and MoM modeling," *IEEE Trans. Microwave Theory Tech.*, vol. 45, pp. 1981-1985, Oct. 1997..

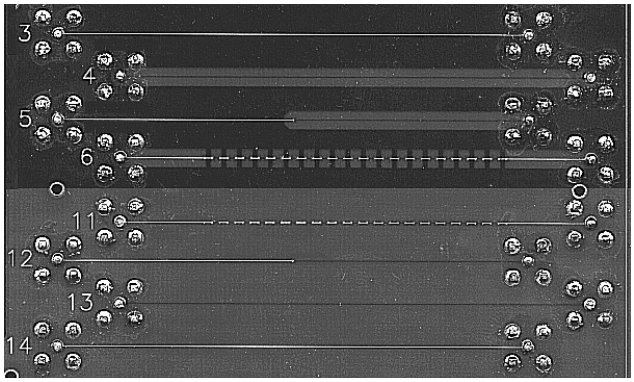

Figure 4 - PCB under test

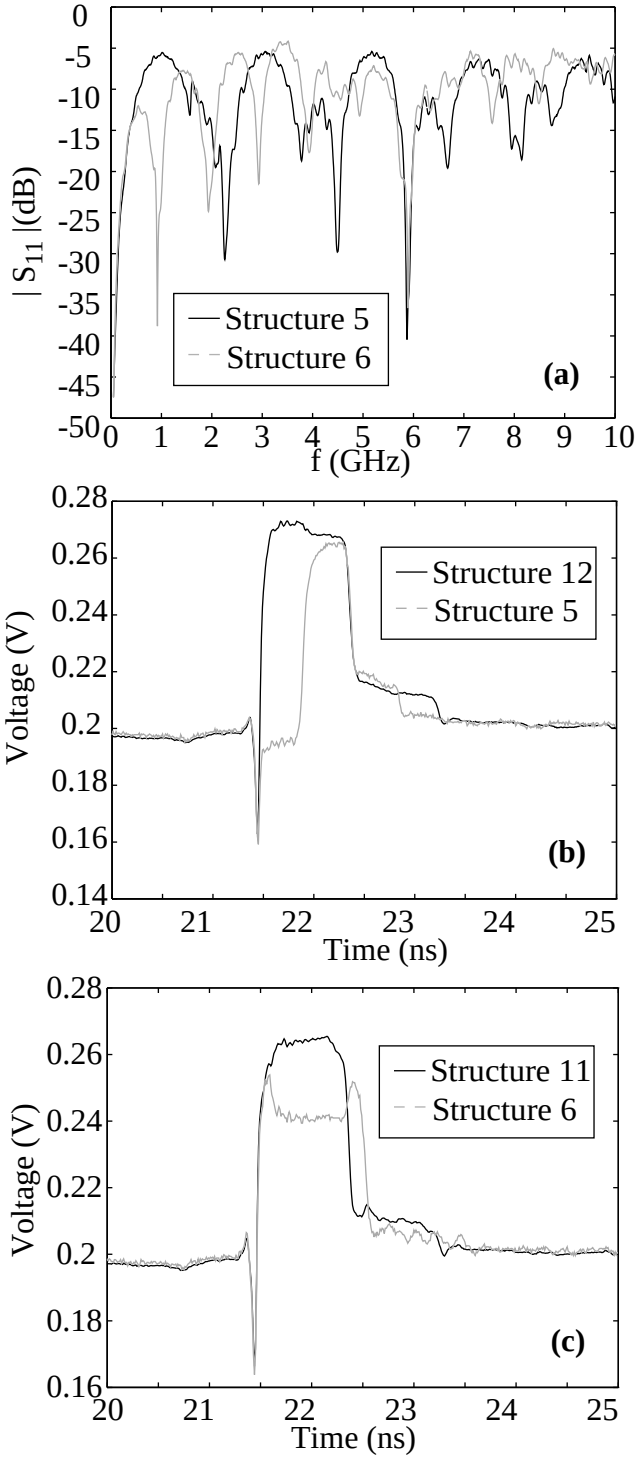

Figure 5 - Experimental results: (a) S_{11} parameters, (b) reflection waveform for single microvia, (c) reflection waveform for the microvia daisy chain